THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL J. BURNS,
PAUL R. DE LA HOUSSAYE, GRAHAM A. GARCIA,
STEPHEN D. RUSSELL, STANLEY R. CLAYTON,
and ANDREW T. BARFKNECHT

Appeal No. 96-1075
Application 08/041,737[1]

ON BRIEF

Before MARTIN, BARRETT, and HECKER, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed April 1, 1993, entitled "Monolithic Integrated High-TC Superconductor-Semiconductor Structure."

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 2, 4-21, 52-57, and 59-84.

We reverse.

BACKGROUND

The disclosed invention is directed to a monolithic integrated superconductor-semiconductor structure. Superconducting devices have much higher theoretical limits for speed than semiconductor devices; however, semiconductor devices perform certain functions better. Thus, there has been incentive to combine both high temperature superconductor (HTS) and semiconductor devices on the same chip to exploit the advantages of each technology.

One obstacle is that "HTS materials are very weakly bound chemically, and are therefore easily decomposed (often into elemental copper and other metals) by direct contact with semiconductors" (specification, page 5). Elemental copper diffuses very fast through semiconductors. "Copper forms a deep electronic trap in Si, Ge, and GaAs, and even at part per million levels it destroys the very properties of the semiconductor which allow it to be used to make

transistors and integrated circuits." (Specification, pages 5-6).

The disclosed invention solves the problem in several ways: (1) "by using a common substrate such as sapphire . . . for the fabrication of both the superconductive and the semiconductor sections of the monolithically integrated structure, direct growth of an oxide superconductor atop a semiconductor is avoided" (specification, page 10); (2) "the use of a protective layer prevents contamination of the semiconductor section during subsequent HTS processing" (specification, pages 10-11); and (3) "[w]hen sapphire is the substrate for both the HTS and the semiconductor parts of the integrated circuits, Cu does not diffuse through the substrate from the HTS devices into the semiconductor structures" (specification, page 11), which reduces the total area of the integrated circuit which must be protected.

Claim 52 is reproduced below.

> 52. A monolithic integrated structure comprising:
>
> an insulating substrate;
>
> a semiconductor region formed on said substrate, said semiconductor region comprising a semiconductor material;

a barrier layer resistant to diffusion of dopants and traps on top of said semiconductor region; and

a superconductor region formed on said substrate, said superconductor region comprising a first superconducting material.

The examiner relies on the following prior art:

U.S. Patents

Gurvitch et al. (Gurvitch)	4,837,609	June 6, 1989
Calviello et al. (Calviello)	5,164,359	November 17, 1992
Yamazaki	5,212,150	May 18, 1993 (filed February 16, 1990)
Sunami et al. (Sunami)	5,266,815	November 30, 1993 (filed April 6, 1992)

Japanese Laid-Open Patent Applications (Kokai)[2]

Nishio	63-276283	November 14, 1988
Mogani	64-35974	February 7, 1989
Aoki et al. (Aoki)	64-86576	March 31, 1989
Ota	1-241875	September 26, 1989

Claims 2, 4-9, 12-14, 16, 52-56, 59-81, and 83 stand rejected under 35 U.S.C. § 103 as being unpatentable over Calviello, Aoki, and Sunami.

Claims 10, 11, 17, and 18 stand rejected under 35 U.S.C. § 103 as being unpatentable over Calviello, Aoki, and Sunami, further in view of Ota and Mogani.

Claims 15, 19-21, 82, and 84 stand rejected under 35 U.S.C. § 103 as being unpatentable over Calviello, Aoki, and Sunami, further in view of Gurvitch and Yamazaki.

Claim 57 stands rejected under 35 U.S.C. § 103 as being unpatentable over Calviello, Aoki, and Sunami, further in view of Nishio.

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[2] Translations of these references have been prepared by the S.T.I.C. Translations Branch of the United States Patent and Trademark Office and accompany this decision.

We refer to the Final Rejection (Paper No. 8) (pages referred to as "FR__") and the Examiner's Answer (Paper No. 19) (pages referred to as "EA__") for a statement of the Examiner's position and to the Appeal Brief (Paper No. 18) (pages referred to as "Br__") and the Reply Brief (Paper No. 20) pages referred to a "RBr__") for a statement of Appellants' arguments.

OPINION

Grouping of claims

Because we reverse the rejections, there is no need to straighten out the Examiner's grouping of the claims.

Claim interpretation

Although the outcome of the appeal does not depend on claim interpretation, there are several matters of claim interpretation which merit discussion.

First, we agree with Appellants' arguments (Br16-20) that the Examiner erred in stating (at FR7) that the limitations of "resistant to diffusion of dopants and traps," "for preserving the semiconducting properties of said semiconductor region during formation of said

superconductor region," "prevents oxidation of said semiconductor region," and "protecting said semiconductor region from contamination during formation of said superconductor region" are functional and not entitled to patentable weight unless expressed in means-plus-function format. The limitations recite functional characteristics or properties of the "barrier layer" in claim 52 and the "layer in contact with and overlying said semiconductor region" in claims 61 and 66; thus, this is not a case where there is no structure recited to support the function. Functional language supported by structure does not have to be recited in means-plus-function format. The noted limitations are entitled to patentable weight. It appears that the Examiner has addressed the limitations in the rejection despite saying that they are not entitled to weight.

Second, there is a question whether claims 61, 66, 71, and 76 contain process limitations and to what extent the Examiner afforded patentable weight to such limitations. As noted by Appellants (Br20), the Final Rejection states that regarding "claims 22-25, the process limitation of when the

superconductor region is formed is given no patentable weight in claims drawn to structure of the final product" (FR7). However, claims 22-25 have been canceled and did not contain such limitations. Claims 61, 66, 71, and 76 recite: "a layer . . . for preserving the semiconductor properties . . . during formation of said superconductor region" (claim 61); "a layer . . . protecting said semiconductor region from contamination during formation of said superconductor region" (claim 66); "means . . . for protecting said semiconductor region from contamination during formation of said superconductor region" (claim 71); and "means . . . for preserving the semiconducting properties . . . during formation of said superconductor region" (claim 76). Appellants argue that "Applicants' recitations of the function performed by the recited layer of preserving the semiconducting properties and protecting from contamination are structural, not product-by-process" (Br21).

Since the layer or means performs the function or has the property of "preserving" or "protecting" the semiconductor region "during formation of said

superconductor region," it is implied that the layer or means is formed before the superconductor region. The order of putting down the barrier layer and the superconductor results in different devices; i.e., a device where the barrier layer is formed after forming the superconductor is different than a device where the barrier layer is formed before forming the superconductor because the semiconductor would be contaminated when the barrier layer is formed last. Further, the order precludes a device where the layer is deposited on top of the semiconductor and superconductor. Thus, claims 61, 66, 71, and 76 require the layer or means to be deposited before the superconductor.

By comparison, claim 52 does not contain any limitations about the "barrier layer" preserving or protecting "during formation of said superconductor region." The order of the limitations in claim 52 do not constitute an order of manufacture; i.e., the fact that the "barrier layer" is recited before the "superconductor region formed on said substrate" does not imply that the barrier layer is constructed before the superconductor region. The "barrier layer" can be formed before or after the superconductor

region. The "resistant to diffusion of dopants or traps" limitation simply recites a property or capability of the "barrier layer" material. To indicate how broad claim 52 is, claim 52 would be met by adding a passivation layer of silicon nitride on top of the semiconductor and HTS regions in Calviello as shown at 14 in Aoki; however, this rejection is not before us.

Third, the limitations of "a semiconductor region formed on said substrate" and "a superconductor region formed on said substrate" exclude forming the semiconductor in bulk silicon. However, the "formed on" limitation does not require the semiconductor or the superconductor to be formed directly on the substrate. As indicated by claim 53, for example, a buffer layer may be interposed between the substrate and superconducting material. In view of this, we agree with the Examiner that "formed on said substrate" does not require the semiconductor region and the superconductor region to be formed on distinct separate areas of the substrate, but broadly admits of the interpretation that the superconductor lies atop the semiconductor. Appellants' arguments in support of the argument that "the reasonable

interpretation of the claims is that the superconductor region and the semiconductor region do not lie atop each other and are distinct substrate regions on different substrate locations" (RBr3-4) do not address the effect of the claimed buffer layer on the claim interpretation. Limitations are not read into the claims during prosecution. See In re Zletz, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (claims are given their broadest reasonable interpretation during examination: "The reason is simply that during patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed.").

Fourth, the limitations of a "layer in contact with and overlying said semiconductor region" (claims 61 and 66) and "means in contact with and overlying said semiconductor region" (claims 71 and 76) do not require that the layer or means completely cover "all" the semiconductor region. The recited functions of "for preserving the semiconducting properties" (claims 61 and 76), "protecting . . . from contamination" (claim 66), and "for protecting . . . from contamination" (claim 71) do not require total protection.

Thus, the isolation film 3 of Sunami, although covering only part of the surface of the semiconductor, is considered to meet the limitation of "a barrier layer resistant to diffusion of dopants and traps on top of said semiconductor region" as recited in claim 52 and the layer and means limitations in the last subparagraph of claims 61, 66, 71, and 76. Sunami does not, however, disclose an insulating substrate.

Obviousness

The Examiner concludes (EA8):

> It would have at the very least been obvious to one skilled in this art to form the active semiconductor layer 108 or 124 of Calviello et al. on a buffer layer 106 or 116 prior to the formation of the high temperature superconductor (HTS) layer 110 or 120 of Calviello et al. on a buffer layer 106 or 118 as shown by Aoki et al. so that a SiO_2 film would cover the active semiconductor layer 108 or 124 and to utilize a barrier layer made of Si_3N_4 on the SiO_2 film or directly on the active semiconductor layer 108 or 124 to prevent diffusion of the constituents of the high temperature (HTS) layer 110 or 120 and to prevent the deterioration of the electrical characteristics of the semiconductor layer 108 or 124 as taught by Sunami et al.

As we understand the rejection, the Examiner proposes to modify Calviello by three steps: (1) interchanging the order of depositing the superconductor 120 and the

semiconductor 124, because Aoki discloses the superconductor deposited on the semiconductor and, hence, deposited after the semiconductor; (2) depositing the superconductor 120 on top of the semiconductor 124, because Aoki discloses the superconductor deposited on the semiconductor; and then (3) interposing a barrier layer between the semiconductor 124 and the overlying superconductor layer as taught by Sunami. The Examiner's proposed combination produces vertically arranged layers of, from bottom to top, an insulating substrate, a semiconductor region, a barrier layer, and a superconductor region. This is a different arrangement from the disclosed invention where the semiconductor region and the superconductor region occupy different areas on the substrate and do not overlie each other. However, as discussed in the claim interpretation section, the independent claims are broad enough to encompass the Examiner's proposed combination.

Some statements in the Response to Argument section of the Examiner's Answer suggest that the rejection would keep the same physical layout of Calviello with the superconductor and the semiconductor regions spaced apart

from each other on the substrate instead of on top of each other as taught by Aoki and Sunami, e.g., EA16, lines 5-7, responding to Appellants' arguments that "formed on the substrate" does not include vertically arranged layers. These statements are inconsistent with the teachings of the references. Both Aoki and Sunami show the superconductor on top of the semiconductor since the semiconductor is formed in the silicon substrate. The reason for the silicon oxide layer 17 in Aoki and the isolation films 3 in Sunami is to separate the superconductor on top of the semiconductor. Sunami teaches using a barrier layer only when the superconductor overlies the semiconductor, not when the superconductor region is distinct from the semiconductor region, which is Appellants' disclosed invention. Thus, we interpret the Examiner's rejection as requiring stacking the superconductor on the semiconductor in Calviello. This is consistent with other statements, such as (EA16): "Even if the high temperature superconductor layer 110 or 120 of Calviello et al. is atop the active semiconductor layer 108 or 124, both layers are <u>still formed on the same ceramic substrate</u>."

Appellants argue that the Examiner erred in concluding that it would have been obvious to stack the HTS on the semiconductor in Calviello (Br13-14):

> Moreover, if one were to modify Calviello per the teachings of Sunami, the resultant structure would have an HTS layer 110 overlying the region 108 and separated from it by Sunami's barrier film 3 and/or barrier electrode 7. The ability to lattice match the HTS layer 110 to the substrate 104 would be completely lost due to the presence of the intervening film 3 and/or barrier electrode 7. . . . The fundamental purpose and basic principles upon which Calviello is purported to operate would thus be destroyed by combining it with Sunami/Aoki as suggested by the Examiner.

We agree with Appellants' argument. Stacking the HTS on top of the semiconductor is contrary to the intended purpose of lattice constant matching the HTS to the substrate and, for this reason, the reasoning in the rejection based on modifying Calviello must fail.

While Aoki and Sunami disclose stacking a superconductor on top of a semiconductor, they do not disclose the claimed "insulating substrate"; thus, the rejection is dependent on the combination with Calviello which shows a sapphire substrate. The Examiner states in the Response to Arguments that "Aoki et al. and Sunami et al. do not teach the silicon bulk substrate may be formed on

an underlying substrate; however, it was well known in this art to form silicon on sapphire (SOS) or silicon on insulator (SOI) structure" (EA18). The rejection does not incorporate this finding of what was well known. Aoki and Sunami are not sufficient to support the rejection.

We conclude that the Examiner has failed to establish a prima facie case of obviousness. The rejection of claims 2, 4-9, 12-14, 16, 52-56, 59-81, and 83 is reversed. The references to Ota, Mogani, Gurvitch, Yamazaki, and Nishio do not cure the deficiency with respect to the rejection of the independent claims. Accordingly, the rejections of claims 10, 11, 15, 17-21, 57, 82, and 84 are reversed.

CONCLUSION

The rejections of claims 2, 4-21, 52-57, and 59-84 are reversed.

REVERSED

JOHN C. MARTIN Administrative Patent Judge	)	
LEE E. BARRETT Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART N. HECKER Administrative Patent Judge	)	

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